Channel Constrained Metalization Patterning of

Reflective Backplane Electrodes for Liquid Crystal-on-Silicon Displays

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Abstract

Channel Constrained Metalization (CCM), which employs photoresist patterning to confine electroless metal deposition to selected regions, is an inexpensive alternative to metal sputtering or evaporation. Using CCM we deposited arrays of square nickel electrodes up to one micron in thickness and between 11 μm and 44 μm on the side. Gaps between the electrodes ranging from 1 μm to 4 μm were successfully patterned. In preliminary experiments, we have already achieved a reflectivity of up to 94% and an r.m.s. surface roughness of 3.3 nm evaluated on a pixel size (20 μm square) area.

Introduction

Liquid Crystal on Silicon[1-6] (LCOS) displays have the potential for a reflective active matrix display combining low cost, small size (a total area of a few cm^2), high resolution (XVGA, HDTV), high speed and color capability. The backplane of this type of display consists of a CMOS silicon chip which not only features an array of highly reflective pixel electrodes with large fill factor (>90% feasible) on its surface, but also integrates the display drivers. The thin liquid crystal layer of an LCOS display is sandwiched between the silicon backplane and a transparent top substrate providing a common transparent ITO electrode for all pixels.

LCOS displays target a wide range of applications such as head-mounted displays for virtual reality, training simulators or information display, projection display, real time holography, optical data storage and optical computing. The potential advantages of LCOS displays are: (1) their high speed and excellent image quality resulting from the high carrier mobility of crystalline silicon and the low capacitances of its compact configuration, and (2) the low cost and ready access to production facilities provided the LCOS backplanes are designed such that they can be manufactured in standard CMOS fabrication services without process modifications.

Silicon chips implemented in standard CMOS fabrication services require considerable post-processing before they become useful LCOS backplanes. Their rough surface topography must first be planarized. Then via holes must be etched through the surface passivation layer to establish electrical contact with the on-chip pixel drivers. And lastly, an array of flat, highly reflective electrodes with large fill factor must be laid out on the planarized surface.

This last step is usually achieved by either evaporation or sputtering of aluminum or chrome, usually on a surface that has been planarized by an additional oxide deposition followed by chemical-mechanical polishing (see for instance ref. 7). However, these methods require access to costly equipment and result in a highly complex, low yield process which significantly increases the overall device cost.

We have therefore sought to identify an electrode patterning process that produces devices with high quality and yield while
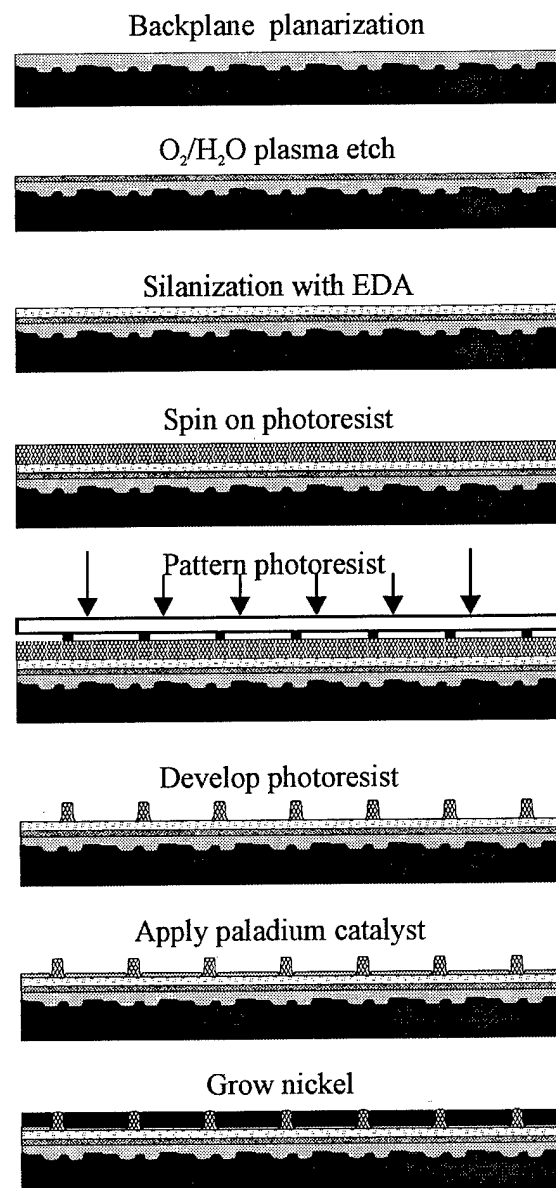
requiring only inexpensive equipment and moderate manpower. Furthermore, these processes should be feasible as automated batch jobs. The results of very recent experiments lead us to conclude that Channel Constrained Metalization[8-10] (CCM) based on electroless plating meets these criteria. This technology has few, readily controlled parameters and requires only a fraction of the investment and expertise needed for alternative approaches.

Experiments

The substrate on which the metal mirrors of an LCOS display must be patterned depends on the method chosen to planarize the silicon backplane. For example, Huang et al.[7] thermally grow additional SiO_2 on the chip surface, which they subsequently planarize by CMP. We prefer a planarization technology that avoids the complexity and capital investment associated with CMP, and instead use a commercially available planarization resin (Dow Chemical XU71918.35™) for low temperature spin-on planarization. What we establish in this work is that it is possible to pattern highly reflective, flat electrodes on top of this polymer using CCM.

The process we have established is shown in Fig. 1. As a demonstration, we spin-coated a silicon wafer with an approximately 2 µm thick layer of XU71918.35™. Next, this polymer film was coated with an N-(2-aminoethyl)3-amino-propyltrimethoxysilane (EDA) monolayer which was then baked to chemisorb the EDA to the planarization polymer. For better adhesion, this step may be preceded by a brief O_2/H_2O plasma etch step, which raises the density of hydroxyl groups at the surface and causes the silane to bind more firmly to the planarization polymer.

We then spin-coated the monolayer with a commercial photoresist (Shipley S1813™), patterned by contact lithography and developed the resist, removing it in areas exposed to UV light and baring the underlying silane mono-layer. With proper exposure and development schedule, no significant scumming is observed. The entire substrate was subsequently puddled

Backplane planarization

O_2/H_2O plasma etch

Silanization with EDA

Spin on photoresist

Pattern photoresist

Develop photoresist

Apply paladium catalyst

Grow nickel

with a

Fig. 1: CCM process flow

palladium catalyst solution[11]. The catalyst forms a covalent bond to the silane but not to the photoresist. The substrate is then rinsed with de-ionized water and immersed in an electroless nickel plating bath (Shipley Niposit 468™).

The rate of metalization buildup depends only on a few parameters: bath concentration, temperature and time. Catalyst properties only appear to affect the dynamics during the first few minutes of plating. At full bath

concentration and 66 °C temperature, the nickel growth rate is about 125 nm/min. However, in this case, the bath has to be continuously agitated to prevent the formation of hydrogen bubbles at the surface. These bubbles stick to the surface and leave holes in the plating. We chose instead a lower bath concentration and a temperature of 21 °C. The observed plating rate is shown in Fig. 2 and is seen to scale roughly linearly with time after a few minutes.
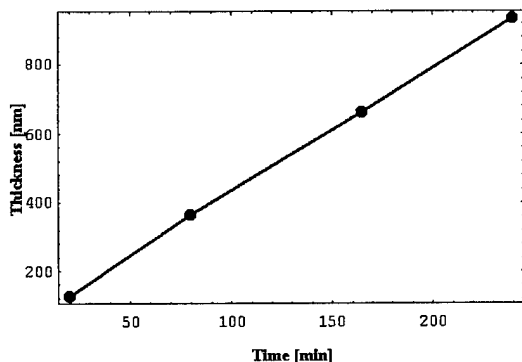

Fig. 2: Nickel plating thickness vs. time at 21 °C

In order to obtain uniform, flat metalization over several cm^2, it is vital to be able to filter both the catalyst and the plating bath. Otherwise impurities and dust carried by either leave intolerable defects in the metalization. This is particularly important as the liquid crystal layer in LCOS devices is only 1-2 µm thick. Our experiments show conclusively that both bath and catalyst can be filtered with 0.2 µm PTFE filters, and that in this case the metalization rate is reduced only in the initial phase during which nickel binds to the palladium particles. While filtering reduces the nickel thickness after one hour of plating by about 10%, it allowed us to achieve high reflectivity (>94%) metalization up to 1 µm thick in preliminary experiments. On a 700 nm thick nickel layer, we measured an r.m.s. surface roughness (20 µm square area) of 3.3 nm and a peak-to-peak roughness of 37 nm.

In Fig. 3, we show optical microscope images of part of a VGA size array of pixels 22 µm on the side with 2 µm gaps to adjacent electrodes. Fig. 3a shows the result of photoresist patterning (prior to plating), and Fig. 3b shows the result after metalization. Fig. 4 shows an AFM scan of

a 22 µm electrode after metalization. We have also produced 11 µm electrodes with 1 µm gap and 44 µm electrodes with 4 µm gap.
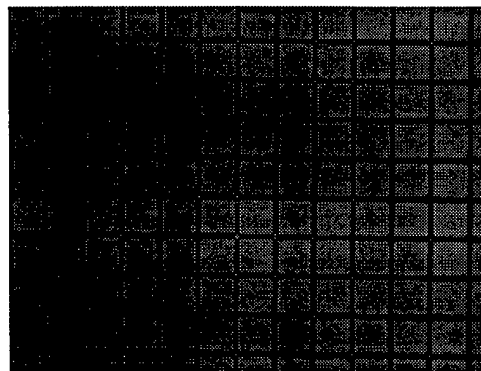

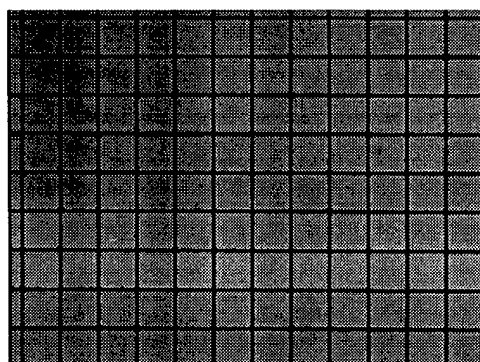Fig. 3a: Part of a VGA size pixel array after photoresist patterning and prior to plating.

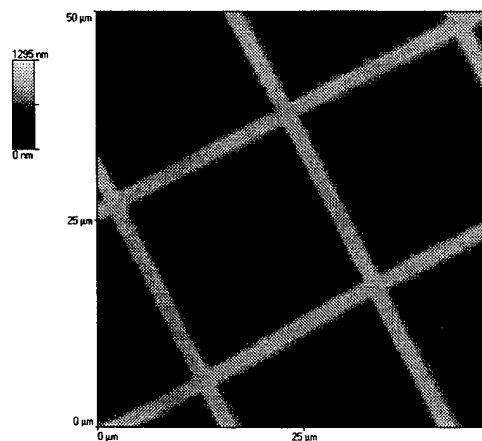Fig. 3b: Part of a VGA size pixel array after photoresist patterning and nickel plating

Fig. 4: AFM image of a 50 µm square area. The metalized electrodes are 22 µm on the side, with a 2 µm wide photoresist spacer between pixels.

Discussion and Summary

Using Channel Constrained Metalization we have patterned arrays of flat, high reflectivity nickel electrodes for LCOS display backplanes. The resulting pure nickel electrodes feature a high broadband reflectivity (>94%) and can be built up to a thickness exceeding 1 μm. We have patterned electrodes with nearest neighbor spacing as narrow as 1 μm and achieved an r.m.s surface roughness of 3.3 nm on a 20 μm square area in preliminary experiments. A related electroless plating process, which will be reported elsewhere, can be used to contact the pixel drivers on the silicon backplane with the reflective electrodes, filling the via holes completely. This approach has the potential for backplane electrodes without the uneven topography arising from the via holes underneath, as is commonly encountered in alternative electrode patterning approaches. The low complexity and cost of this process make it extremely attractive compared to sputtering and evaporation. Further improvements of surface roughness and reflectivity are possible by process optimization and by choosing a smaller particle size Pd catalyst[12].

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